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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,386	09/28/2001	Len Schultz	42390P5728	5088

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EXAMINER	
LE, DIEU MINH T	

ART UNIT	PAPER NUMBER
2114	5

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/966,386	Applicant(s) SCHULTZ ET AL.	
	Examiner Dieu-Minh Le	Art Unit 2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 4-5, 7-8, 10-11 are rejected under 35 U.S.C. § 102(a) as being anticipated by Applicant's admitted prior art US 2003/0074601 A1 "BACKBROUND OF THE INVENTION" hereafter referred to as Prior Arts).

As per claim 1:

Prior Arts explicitly teaches:

- A method comprising of:

- using processor implementation-specific instructions [col. 1, lines 53-56] to save a processor state [col. 1, [0002], lines 11-15] in a system memory when a machine check error is generated by a processor [col. 1, [0002], lines 9-10];

- attempting to correct the error [col. 1, [0002], lines 1-2) using processor implementation-specific instruction [col. 1, [0001], lines 7-10, and [0002], lines 9-11];

- transferring control from processor-independent instruction [col. 1, [0002], lines 18-20];

- receiving control from processor-independent instruction [col. 1, [0002], lines 21-24];

- returning [col. 1, [0002], line 14] to an interrupted context [col. 2, [0002], line 15] of the processor by restoring the processor state [abstract, col. 1, [0002],lines 11-16].

This is clearly shown that Prior Art's teaching capabilities are corresponding to Applicant's invention.

As per claims 2, 4 and 5:

Prior Arts further explicitly teaches:

- providing processor error record information obtained using processor implementation-specific instructions [col. 1, [0002], lines 2-4];

- receiving control from processor-independent instruction indicates that the error has been corrected [col. 1, [0002], lines 2-4];

- obtaining an address of a location to save the processor state in the system memory provided by platform-specific instructions [col. 1, [0002], lines 11-15].

This is clearly shown that Prior Art's teaching capabilities are corresponding to Applicant's invention.

As per claims 7-8, 10-11:

Due to the similarity of claims 7-8 and 10-11 to claims 1-2, 4-5; therefore, these claims are also rejected under the same rationale applied against claims 1-2, 4-5. **In addition, all of the limitations have been noted in the rejection as per claims 1-2, 4-5.**

3. Claims 1-20 are rejected under 35 U.S.C. § 102(e) as being anticipated by Klecka et al. (US Patent 6,393,582 hereafter referred to as Klecka).

As per claim 1:

Klecka explicitly teaches:

- A method comprising of:

- using processor implementation-specific instructions [col. 1, lines 53-56] to save a processor state [abstract, col. 1, line 64] in a system memory when a machine check error is generated by a processor [abstract, col. 1, lines 5-10];

- attempting to correct the error (i.e., ECC) [col. 3, line 40) using processor implementation-specific instruction [col. 1, lines 62-64, col. 7, lines 59-64];

- transferring control from processor-independent instruction [col. 2, lines 4-11, col. 9, lines 34-45, and col. 10, lines 38-52];

- receiving control from processor-independent instruction [col. 2, lines 4-11, col. 9, lines 34-45, and col. 10, lines 38-52];

- returning [col. 2, lines 1-3] to an interrupted context [col. 4, lines 34-39 and col. 4, lines 66 through col. 5,

lines 10] of the processor by restoring the processor state [abstract, col. 1, lines 62 through col. 2, lines 3].

This is clearly shown that Klecka's teaching capabilities are corresponding to Applicant's invention.

As per claims 2-3:

Klecka further explicitly teaches:

- providing processor error record information obtained using processor implementation-specific instructions [col. 3, lines 29-44 and col. 10, lines 53-58];
- attempting to contain the error if a second processor is coupled to the processor by requesting a rendezvous between the processor and the second processor [col. 1, lines 8-10 col. 3, lines 5-44].

This is clearly shown that Klecka's teaching capabilities are corresponding to Applicant's invention.

As per claims 4-6

Klecka further explicitly teaches:

- receiving control from processor-independent instruction indicates that the error has been corrected [col. 2, lines 1-3];

- obtaining an address of a location to save the processor state in the system memory provided by platform-specific instructions [col. 8, lines 61-67 and col. 10, lines 34-35];

- attempting to correct the error using processor implementation-specific instruction is not done if an expected machine check indicator is set [col. 10, lines 50-57 and col. 13, lines 52-58].

This is clearly shown that Klecka's teaching capabilities are corresponding to Applicant's invention.

As per claims 7-13:

These claims are the same as per claims 1-6. The only minor different is that these claims are directed to a **machine-readable medium** instead of the method for using processor implementation-specific instructions [col. 1, lines 53-56] to save a processor state [abstract, col. 1, line 64] in a system memory when a machine check error is generated by a processor as described in claims 1-6. However, it would have been obvious to

one having ordinary skill in the art at the time the invention was made to realize that the **machine-readable medium** is a necessary item for computer system, more specifically, for processors or central processing units (CPUs) capability. Since the computer processing system obviously needs a means for instruction or code means resided within the machine-readable storage medium for performing the data checking, detecting, correcting, validating, storing, receiving, transmitting operation via the computing operation hardware and software platform. Therefore, these claims are also rejected under the same rationale applied against claims 1-6.

As per claims 14-20:

These claims are similar to claims 1-6. The only minor different is that these claims introduce:

- first and second machine readable mediums (i.e., master processor and shadow processor units, caches, and memory) [fig. 1, col. 2, lines 66-67];
- error uncorrected [col. 8, lines 24-34];
- halting and rebooting of the CPU [fig. 1-4, col. 6, lines 63 through col. 7, line 3, col. 7, lines 26-38 and col. 7, lines 55-58].

This is clearly shown that Klecka's teaching capabilities are corresponding to Applicant's invention.

Therefore, these claims are also rejected under the same rationale applied against claims 1-6.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (703)305-9408. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703)305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2184

DML
5/28/04